Efficient Modelling of a PCB Transmission Line for High Speed Digital Systems

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***Abstract*—This paper proposes a model of PCB traces for high speed digital systems. The adopted approach involves predetermined geometry using direct discretization of transmission lines. Initially, the proposed methodology involves computing the line propagation delay by employing its geometry with associated empirical equations. The initial procedure paves the way to design a Lattice diagram which depicts multiple reflections that the signal underwent due to impedance mismatches between transmission lines and loads. Subsequent computations of electrical model parameters were further done. Simulation results using Multisim software illustrated a favorable performance with a time delay of 1.42 ns and an equivalent electrical model of 10 lumped LC cells. The time delay between input and output signal obtained from the simulation was approximately 15.152 ns corresponding to the time it took for a transmitted signal to reach a steady state which further signifies good performance of our proposed method.**

Keywords—digital systems, transmission line modelling, PCB traces, signaling, time delay, Lattice diagram

I. INTRODUCTION (*HEADING 1*)

Digital Systems are basically comprised of digital devices interconnected (networked) on a Printed Circuit Board (PCB). Majority of today's electronic appliances/devices ranging from DVD players, computers, radio, cookers, heaters etc. are all made of PCB on which a number of components are soldered. These components on the PCB perform complex activities and render good services to users. As a result of the recent technological evolution, especially the integration of nanotechnology and the increase in device operation frequency beyond 100 MHz, digital systems have faced numerous challenges that were previously overlooked and ignored. The bottom line being the ineffective transmission of 0s and 1s that form the basis of effective communication among devices on the same PCB [1]–[3]. Kung and Chuah [4] stressed that the increase in operating frequency of devices in excess of 100MHz and switching speed of digital devices around nanoseconds can cause electromagnetic interference, alter parameters of components and create inadvertent radiation that becomes a major concern, affecting the integrity of a system. Hall *et al*. [1] further argued that for systems that operate at high frequency, conductors are to be considered as transmission lines with parameters properly estimated to account for the level of noise and timing induced.

Furthermore, Mandic [5] elucidated that conducting an electromagnetic analysis of digital systems operating at high frequencies is mandatory. Dally and Poulton [6] indicated that noise beyond a threshold can be completely rejected by any digital system and this situation can easily occur with high speed digital systems if proper care is not taken at the conception level. They further explained that the system level engineering problems can be grouped in four categories including: power distribution, noise management, signaling and timing/synchronization. Power distribution deals with the sharing of a certain Direct Current (DC) level across component of the same system. Noise management deals with the quantification and measures put in place to reduce or cancel noise totally. Signaling deals with the methods of conveying the signals over a transmission line at maximum speed and with minimum power. Timing deals with sequencing of communication among modules and synchronization help coordinate the operation of two systems using different time basis [6].

To address most of the digital system issues enumerated above, knowledge of the model of the transmission line is highly necessary and indispensable. In relation to digital system reliability, the evident increase in the speed of digital systems has paved the way for some challenging factors such as noise, power distribution, signaling and timing. Consequently, without an effective model for PCB transmission, the factors enumerated above cannot be validated properly and this leads to the design of ineffective or unreliable digital systems.

This paper therefore seeks to propose a model of PCB traces for high speed digital systems. Our proposed method utilizes an

approach that involves predetermined geometry using direct discretization of transmission lines. The major contributions of this paper can be summarized as follows.

- A model of PCB traces has been proposed for high speed digital systems by utilizing an approach that involves predetermined geometry using direct discretization of transmission lines.
- The proposed methodology involves computing the line propagation delay by employing its geometry with associated empirical equations and designing a Lattice diagram which depicts multiple reflections undertaken by a signal.
- A series of simulations has been conducted using Multisim software to verify the effectiveness of the proposed method.

The rest of this paper is organized as follow. Section II describes related works to the study. Section III elaborates on the details of our proposed PCB model. Simulation results are presented and analyzed in Section IV. Finally, Section VI concludes this paper.

II. Related Works

Many models of PCB transmission lines have been developed in previous studies. Kung and Chuah [4] proposed a structural approach to derive a system level equivalent circuit model for digital PCB. Park *et al*. [7] worked on the modelling of thin and flexible magnetic sheet, commonly used in modern digital systems. Sayegh *et al*. [8] estimated the radiated emissions from PCB traces. Additionally, Yook *et al*. [9] developed a 3D electromagnetic field analysis tool to estimate system level noise and optimize placement of decoupling capacitors in order to minimize noise fluctuation on the PCB. The effect of electromagnetic noise coupling on PCB transmission line was further modelled by Xu and Mazumder [10] who developed a new technique known as finite difference quadrature (FDQ). Furthermore Liang *et al*. [11] quantified the effect of dielectric and resistive losses by proposing a number of modelling approach for high speed transmission lines on PCB.

A general summary of major methods used to model high speed interconnects on PCB is provided in [12], [13]. They explained that the exiting macro-modelling techniques include numerical convolution of transfer function [14], method of characteristic [15], [16], basis function macro-models, compact finite difference-based approximation [17], integrated congruence transform [18] and finally direct discretization of transmission line which is of high interest in this paper. In the direct discretization technique, transmission lines are represented as series of cascaded lumped sections representing an infinitesimal portion of the line often denoted Δz. This method best applies to short transmission lines similar to those on PCB and this is the fundamental reason why it has been selected for the developed model of PCB in this study.

Our review in literature shows that high speed can influence signal propagation over PCB in several manners. Most effects dealt with in the literature are signal degradation, attenuation, crosstalk, skin effect, overshoot and undershoots. However, the timing related effect like delay, ringing and reflection have not been sufficiently modelled, despite their detrimental effects on the overall performance of the PCB. Moreover, the limitation of direct discretization of transmission line for not being accurate in modelling long transmission line has also limited its exploitation in modelling PCB traces though the method is very efficacious and involve less complexity in modelling short transmission lines like those encountered on PCBs. Inspired by the enumerated open issue, this study investigates the reflection and ringing effect on a PCB transmission line modelled with the direct discretization using Lattice diagram. The study further develops and simulates an electrical model of the line under consideration using Multisim software to accurately provide an estimate of the accrued delays.

III. Methodology

A simplistic high-speed digital system made of two components C_1 and C_2 communicating through a transmission line made of four-layer stack-up as depicted in Fig. 1 has been considered. It is assumed that component C_1 has a characteristic impedance of 40 Ω, an edge rate of 150 ps and a signal swing of 0 to 2V. It is expected that the traces on the PCB should have an impedance of 60 Ω and be 10 inches long. The insulation material in the PCB is assumed to be FR4 which has a dielectric constant of 4. Furthermore, it is assumed that the receiver capacitance is insignificant and therefore can be neglected. Our aim is to determine the model of the transmission line by looking at the reflection phenomena and the delay accrued for a transmission from C_1 to C_2.

The model of the transmission line with its propagation delay and other parameters will be determined through the following steps:

- Computation of the unknown Height (H) in Fig. 1. that meets the line impedance of 60 Ω
- Estimation of the propagation delay which consists of the time for the signal to propagate from component C_1 to C_2.
- Computation of the wave shape seen at C_2 when the system is driven by C_1.
- Creation of line model.
- Simulation of line model under Multisim software.

A. Computation of Height (H)

Hall *et al*. [1] proposed an analytical model to determine the impedance of the geometry proposed in Fig. 1. It must be noted that the lines are essentially microstrip and the model is presented in (1).

$$Z_{o\_microstrip} = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.48H}{0.8W + T}\right) \quad (1)$$

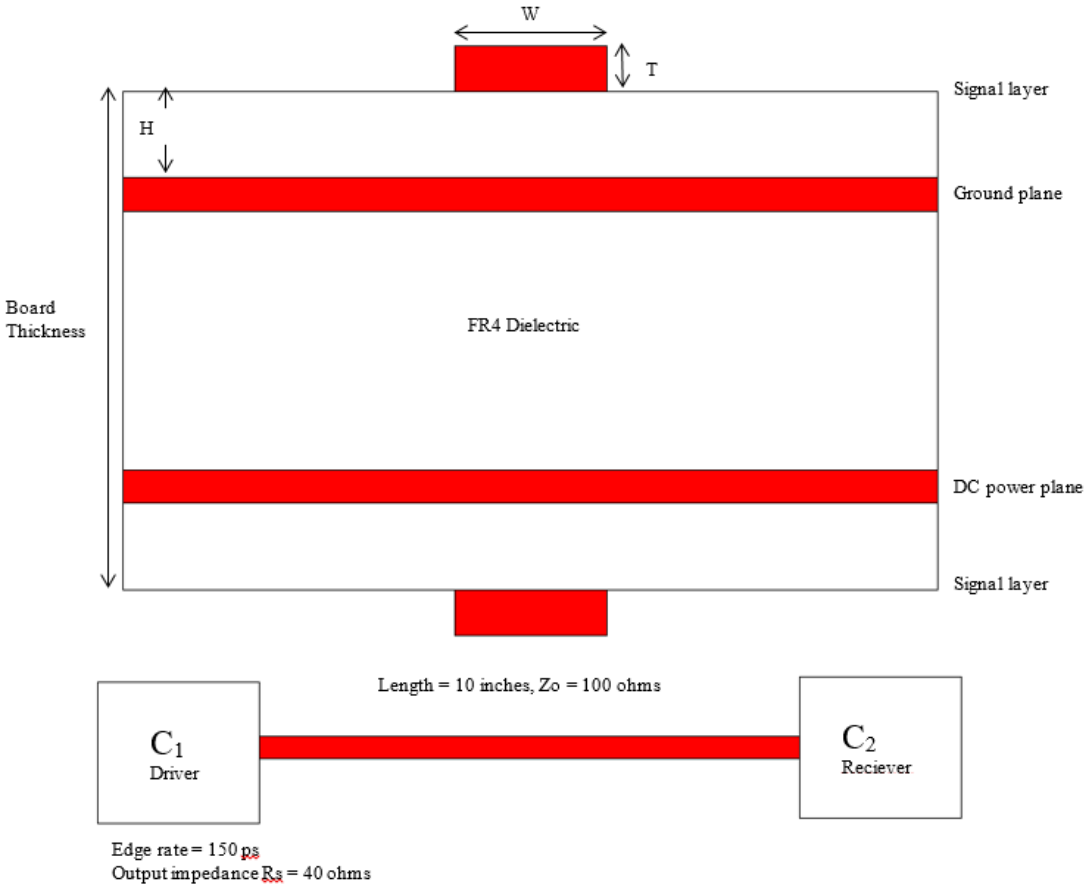


Fig. 1. four-layer stack-up transmission line

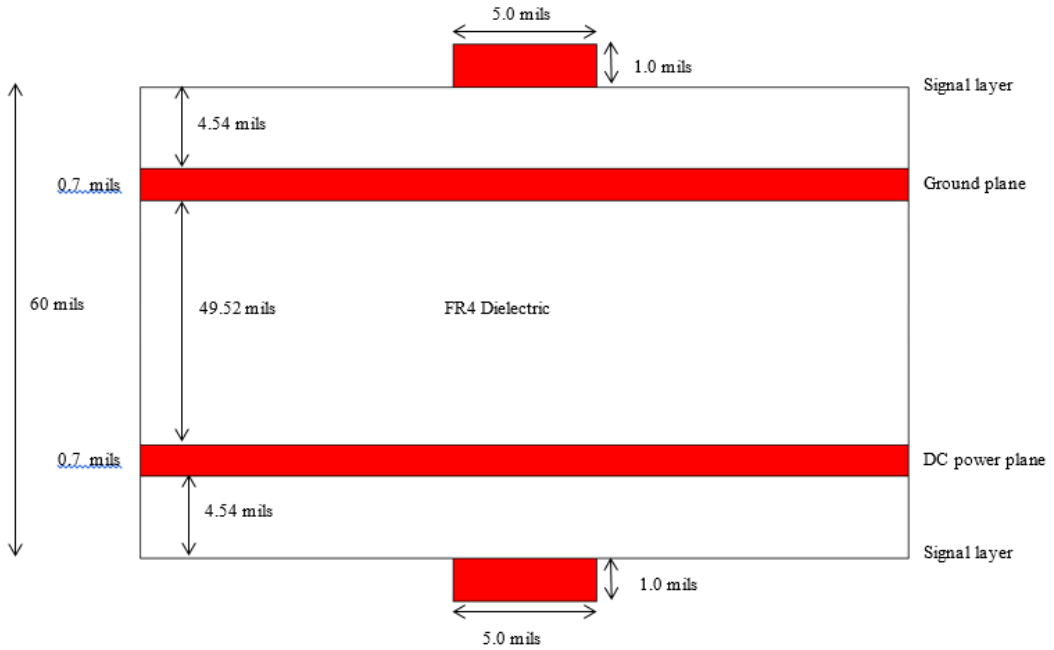


Fig. 2. PCB Stack-up for 100 ohms transmission line

In (1), $Z_{o\_microstrip}$ is the impedance of the microstrip, H is the height between the ground plane and signal layer and W and T are respectively the width and the thickness as illustrated in Fig. 1. ε_r = Relative dielectric constant. T is the standard metal thickness of microstrip layers on a PCB.

$$\ln\left(\frac{5.48H}{0.8W+T}\right)=\frac{\sqrt{\varepsilon_r+1.41}}{87}\cdot Z_{o\_microstrip} \quad (2)$$

$$H=\left(\frac{0.8W+T}{5.48}\right)\cdot e^{\frac{\sqrt{\varepsilon_r+1.41}}{87}Z_{o\_microstrip}} \quad (3)$$

$$H=\left(\frac{0.8W+T}{5.48}\right)\cdot e^{\frac{\sqrt{\varepsilon_r+1.41}}{87}\times 60} \quad (4)$$

$$H=4.54 \text{ mils} \quad (5)$$

Based on the values obtained, the final line geometry is illustrated in Fig. 2.

B. Calculation of Propagation Delay

Hall *et al*. [1] proposed the fundamental model for calculating propagation delay and propagation velocity as shown in (6) and (7). This equation will be applied to determine the delay of propagation from component C_1 to component C_2.

$$TD=\frac{x\sqrt{\varepsilon_r}}{C} \quad (6)$$

$$\vartheta=\frac{C}{\sqrt{\varepsilon_r}} \quad (7)$$

Where ϑ is the propagation velocity, in meters/second, TD = time delay for a signal to propagate down a transmission line of length x; x = length of the transmission line, in meters and C = speed of light in a vacuum (3 × 108 m/s).

Owing to the fact that the lines adopted are microstrip rather than stripline, there is a contact with air that plays in determining the effective dielectric. The effective dielectric is a weighted sum of the dielectric of the two materials the conductor is in contact with. The models of (8) and (9) were then used in this regard to compute the effective dielectric ε_e as follows.

$$\varepsilon_e=\frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left(1+\frac{12H}{W}\right)^{-2}+G-0.217(\varepsilon_r-1)\frac{T}{\sqrt{WH}} \quad (8)$$

$$G=\begin{cases}0.02(\varepsilon_r-1)\left(1-\frac{W}{H}\right)^2 & \text{for } \frac{W}{H}<1\\ 0 & \text{for } \frac{W}{H}>1\end{cases} \quad (9)$$

Since W/H = 5/4.54 > 1.0, then G = 0. Therefore,

$$\varepsilon_e=\frac{4.0+1}{2}+\frac{4.0-1}{2}\left(1+\frac{12\times 4.54}{5.0}\right)^{-2}+0-0.217(4.0-1)\frac{1.0}{\sqrt{5.0\times 4.54}} \quad (10)$$

$$\varepsilon_e=2.8 \quad (11)$$

The propagation velocity is determined using (7) as follows

$$\vartheta=\frac{C}{\sqrt{\varepsilon_e}}=\frac{3.0\times 10^8 \text{m/s}}{\sqrt{2.8}} \quad (12)$$

$$\vartheta=1.8\times 10^8 \text{m/s} \quad (13)$$

The time delay for the signal to propagate down the 10-in. line connecting C_1 and C_2 is then calculated using (6).

$$TD=\frac{x\sqrt{\varepsilon_r}}{C}=\frac{10.0 \text{ in.}}{1.8 \text{ m/s}}\left(\frac{0.0254}{1.0 \text{ in.}}\right)=1.42 \text{ ns} \quad (14)$$

C. Wave Shape Seen at the Receiver

The Two popular tools have been used to monitor wave shapes of bouncing signals: Bergeron and Lattice diagram. The Bergeron diagram is most applicable in presence of non-linear devices such as diode and transistors. Because of the absence of those devices in the proposed model, a Lattice diagram is used to plot the wave shape at the receiver. The use of the Lattice diagram is based on the determination of the initial voltage launched onto the line and the source and destination reflection coefficient which are calculated with (15), (16) and (17) as follow.

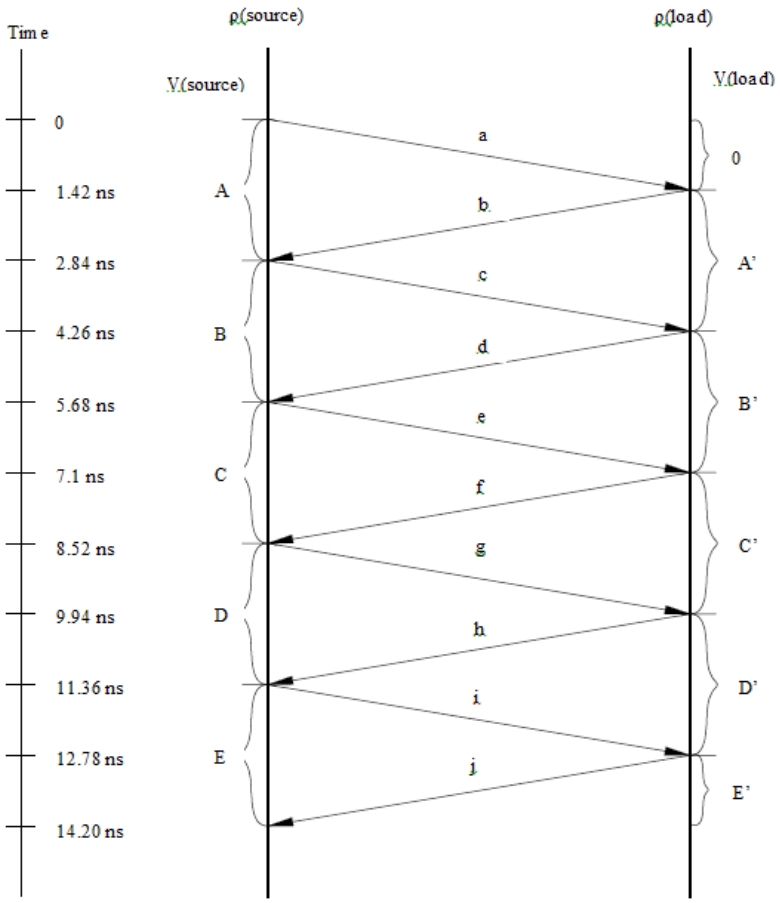
$$V_{initial}=V_{input}\cdot\frac{Z_{o_{PCB}}}{Z_{o_{PCB}}+R_S} \quad (15)$$

$$\rho_{source}=\frac{R_S-Z_{o_{PCB}}}{R_S+Z_{o_{PCB}}} \quad (16)$$

$$\rho_{load}=\frac{R_{load}-Z_{o_{PCB}}}{R_{load}+Z_{o_{PCB}}} \quad (17)$$

where R_S is the buffer impedance of C_1 and R_{load} is the open circuit impedance seen at U_2.

Application: In the case of the network described in Fig. 1,$V_{input}=2V$, $Z_{o_{PCB}}=60\Omega$, $R_S=40\Omega$ and $R_{load}=+\infty$ since the line termination is in open mode.



Legend

$$a = V_{initialV} = 1.2V$$
$$b = a \times \rho_{load} = 1.2V$$
$$c = b \times \rho_{source} = -0.24V$$
$$d = c \times \rho_{load} = -0.24V$$
$$e = d \times \rho_{source} = 0.048V$$
$$f = e \times \rho_{load} = 0.048V$$
$$g = f \times \rho_{source} = -0.0096V$$
$$h = g \times \rho_{load} = -0.0096V$$
$$i = h \times \rho_{source} = 0.0019V$$

$$A = a = 1.2V$$
$$B = A + b + c = 2.16V$$
$$C = B + d + e = 1.968V$$
$$D = C + f + g = 2.0064V$$
$$E = D + h + i = 1.9987V$$
$$A' = A + b = 2.4V$$
$$B' = B + d = 1.92V$$
$$C' = C + f = 2.016V$$
$$D' = D + h = 1.9968V$$
$$E' = E + j = 2.0006$$

Fig. 3. Wave shape at receiver with the lattice diagram

$$V_{initial} = 2 \cdot \frac{60}{60+40} = 1.2V \quad (18)$$

$$\rho_{source} = \frac{40-60}{40+60} = -0.2 \quad (19)$$

$$\rho_{load} = \frac{\infty - 60}{\infty + 60} = 1 \quad (20)$$

Fig. 3 represents a Lattice diagram which is used to show the reflection that the signal has undertaken before reaching a steady state regime. The two vertical lines in the diagram represent respectively, the source and the load with their respective coefficient as estimated in (19) and (20). Reflection occurs as a result of impedance mismatch between the transmission line and the load. A portion of the signal is always reflected as far as the impedances are different; the portion of the signal being reflected is proportional to the reflection coefficient. The diagonal lines between the two vertical lines represent the various reflections between the source and the load. The respective reflection coefficient at various time are marked on the two vertical lines. The lowercase letters represent the magnitude of the reflected signal traveling on the line, the uppercase letters represent the voltages seen at the source, and the primed uppercase letters represent the voltage seen at the load end of the line.

The time step of each reflection is equivalent to the time delay estimated earlier and this presumes that it takes one TD (time delay) for the signal to propagate from one end to the other. The reflection phenomenon continues until the steady state voltage of 2 is reached. The legend explains how the various coefficients on the graph have been calculated.

Fig. 4 summarizes clearly the reflections obtained in the Lattice diagram in Fig. 3. Fig. 4 actually shows the signals at the load and the source side with their respective variations. The shape of the waveforms is similar to a stair-case and the two signal values converge after a duration of about 15.2 ns corresponding to a duration between 10 to 11 times, the TD = (10 x 1.42 = 14.2 ns and 11 x 1.42=15.62 ns). The steady state regime can therefore be considered as starting from the time 15.20 ns. The signal ringing on the line before 15.20 ns, which is mainly due to several reflections can subsequently lead to the occurrence of Inter-symbol interference.

The pattern of reflection illustrated in Figs. 3 and 4 correspond to the case of an undriven transmission line which occurs as far as the source impedance is larger than the line impedance. The next section explains the development of an equivalent electrical circuit to model this transmission line, which will be simulated with Multisim software.

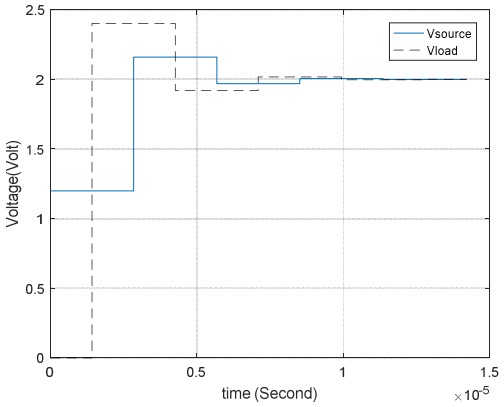


Fig.4. Waveform of voltages at C_1 and C_2

D. Creating an Equivalent Electrical Circuit Model

The equivalent model of the proposed digital system in Fig. 1 can be completely derived from the knowledge of the number of LC segments needed to represent the line with almost the same parameters because it is obvious that practically, an infinite number of elements cannot be represented.

The selection of the finite number of LC cells to be cascaded, is derived from the assertion that: the required minimum number of segments should be cautiously selected so that the time delay of the smallest segment model is lesser than one-tenth of the system rise or fall time as illustrated in (21) [1]. To apply this rule, the velocity determined earlier will be converted to the units of inches/picosecond as in equation (22).

$$N_{segment} \geq 10 \cdot \left(\frac{x}{T_r \vartheta}\right) \quad (21)$$

$$= 10 \cdot \frac{10\text{ in}}{(150 \times 10^{-3}\text{ns})\left(7.04\frac{\text{in}}{\text{ns}}\right)}$$

$$= 9.47$$

$$\vartheta(\text{in/ns}) = \frac{x}{TD} = \frac{10\text{ in}}{1.42\text{ ns}} = 7.04\text{ in/ns} \quad (22)$$

In (22), $\vartheta(\text{in/ns})$ represents the velocity in inches/nanosecond. In equation (21) $N_{segment}$ represents the total number of segments and T_r is edge rate of the driver C_1.

As a result, ten segment of LC cells will be used to develop a precise model of the digital system shown in Fig. 1. With the knowledge of TD and Z_o the equivalent capacitor and inductor values can be extracted as in (23) and (24) as follows.

$$C = \frac{TD}{Z_o} = \frac{1.42\text{ ns}}{60} = 23.7\text{ pF} \quad (23)$$

$$L = TD \cdot Z_o = 1.42\text{ ns} \times 60 = 85.2\text{ nH} \quad (24)$$

Now, the capacitance and inductance per segment

$C_{segment}$ and $L_{segment}$ are calculated as follows.

$$C_{segment} = \frac{\text{length} \cdot C}{N_{segment}} = \frac{10 \text{ in } \times 23.7 \text{ pF/in}}{10} = 23.7 \text{ pF/segment} \quad (25)$$

$$L_{segment} = \frac{\text{length} \cdot L}{N_{segment}} = \frac{10 \text{ in } \times 85.2 \text{ nH/in}}{10} = 85.2 \text{ nH/segment} \quad (26)$$

Fig. 5 shows the equivalent circuit diagram of the transmission line which is made of 10 LC segments, a large resistor of about 10 MΩ is used to model the open circuit at the end of the line. Also, the driving buffer C_1 is represented by a voltage source in series with a source impedance R_1 of 40Ω.

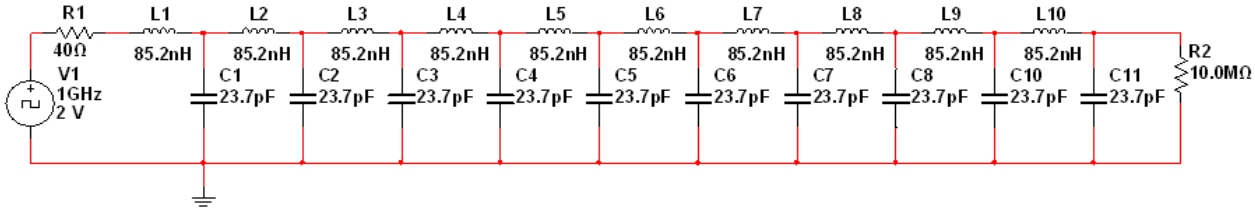
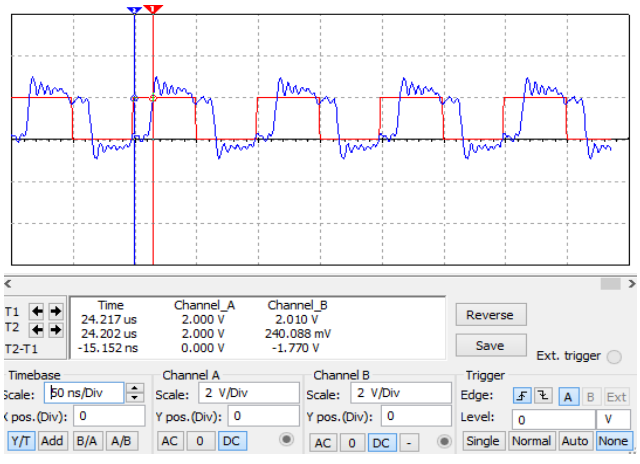


Fig. 5. Proposed equivalent model of the transmission line

IV. Performance Evaluation

The equivalent model presented in Fig. 5 has been constructed and simulated under Multisim software and the simulation results as well as parameters are illustrated in Fig. 6. It can be observed that the output signal is a little deformed as compared to the input signal. The main concern is the delay of the output signal against the input. With reference carefully selected on the two graphs (vertical lines in blue and red), the difference of time which is the delay of the output signal over the input signal is evaluated to be 15.152 ns. This is comparable to the estimated time it took for the system to reach a steady state. Referring to Fig. 4, it can be observed that at 15.152 ns, the system has attained a perfect steady state regime. This further confirms the effectiveness of the model and its capability to predict delays resulting from high speed signal being propagated on PCB traces.



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V. Conclusion

In this paper, we proposed an innovative technique for modelling transmission lines on PCB especially in situations whereby the signals are routed through high speed. Our proposed model which consists of cascaded LC cells is well applicable for short transmission line modelling. The proposed model is also derived from an approach known as direct discretization of microstrip with a predetermined geometry. Reflection phenomena of signals on the transmission line, mainly caused by impedance mismatches was investigated with Lattice diagram. Furthermore, a total of 10 LC lumped network has been cascaded to model the propose transmission line which was evaluated with Multisim simulation software. Simulation results show that the delay between the output and input signal, approximately, 15.152 ns, was in conformity with the estimated time it took for the system to reach steady-state.

In future, further studies in the same direction should explore and investigate the level of intersymbol interference and crosstalk caused by similar disturbances.

References

[1] S. H. Hall, G. W. Hall, and J. A. McCall, *High speed digital system design: a handbook of interconnect theory and design practices*. John Wiley & Sons, Inc., 2000.

[2] M. Adamski and A. Barkalov, *Lecture Notes in Electrical Engineering Volume 79*, vol. 79. Springer-Verlag Berlin, 2011.

[3] Y. Shlepnev, "Modeling frequency-dependent conductor losses and dispersion in serial data channel interconnects," *Simberian Electromagn. Solut.*, pp. 1–12, 2007.

[4] B. Zhong, "Lossy transmission line modeling and simulation using special functions.," University of Arizona, 2006.

[5] R. Achar and M. S. Nakhla, "Simulation of high-speed interconnects," *Proc. IEEE*, vol. 89, no. 5, pp. 693–727, 2001.

[6] A. R. Newton and D. O. Pederson, "Algorithms for the Transient Simulation of Lossy Interconnect," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 13, no. 1, pp. 96–104, 1994.

[7] T. Hu, B. Zhong, S. L. Dvorak, and J. L. Prince, "Application of recursive convolution to transient simulation of interconnects using a hybrid phase-pole macromodel," *IEEE Trans. Adv. Packag.*, vol. 27, no. 4, pp. 603–610, 2004.

[8] B. Zhong, T. Hu, D. Fu, S. L. Dvorak, and J. L. Prince, "Simulation of Complex Interconnects Structures," *Comput. Des.*, vol. 24, no. 8, pp. 1250–1261, 2005.

[9] A. C. Cangellaris, "A new discrete transmission line model for passive model order reduction and macromodeling of high-speed interconnections," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 356–364, 1999.

[10] Q. Yu, J. M. L. Wang, and E. S. Kuh, "Passive multipoint moment matching model order reduction algorithm on multiport distributed interconnect networks," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 46, no. 1, pp. 140–160, 1999.